SPECIFICATION

Please amend paragraph [0001] as follows:

[0001] The present document contains material related to the material of copending, cofiled, ~~U.S. patent applications Attorney Docket Number 100111221-1, entitled System And Method For Determining Wire Capacitance For A VLSI Circuit; Attorney Docket Number 100111227-1, entitled System And Method For Determining Applicable Configuration Information For Use In Analysis Of A Computer Aided Design; Attorney Docket Number 100111228-1, entitled Systems And Methods Utilizing Fast Analysis Information During Detailed Analysis Of A Circuit Design; Attorney Docket Number 100111230-1, entitled Systems And Methods For Determining Activity Factors Of A Circuit Design; Attorney Docket Number 100111232-1, entitled System And Method For Determining A Highest Level Signal Name In A Hierarchical VLSI Design; Attorney Docket Number 100111233-1, entitled System and Method For Determining Connectivity Of Nets In A Hierarchical Circuit Design; Attorney Docket Number 100111234-1, entitled System And Method Analyzing Design Elements In Computer Aided Design Tools; Attorney Docket Number 100111235-1, entitled System And Method For Determining Unmatched Design Elements In A Computer Automated Design; Attorney Docket Number 100111236-1, entitled Computer Aided Design Systems And Methods With Reduced Memory Utilization; Attorney Docket Number 100111238-1, entitled System And Method For Iteratively Traversing A Hierarchical Circuit Design; Attorney Docket Number 100111257-1, entitled Systems And Methods For Establishing Data Model Consistency Of Computer Aided Design Tools; and Attorney Docket Number 100111259-1, entitled Systems And Methods For Identifying Data Sources Associated With A Circuit Design,~~ U.S. Patent Application Number 10/647,597, entitled System And Method For Determining Wire Capacitance For A VLSI Circuit; U.S. Patent Application Number 10/647,595, entitled System And Method For Determining Applicable Configuration Information For Use In Analysis Of A Computer Aided Design; U.S. Patent Application Number 10/647,687, entitled Systems And Methods Utilizing Fast Analysis Information During Detailed Analysis Of A Circuit Design; U.S. Patent Application Number 10/647,594, entitled

Systems And Methods For Determining Activity Factors Of A Circuit Design; U.S. Patent Application Number 10/647,768, entitled System And Method For Determining A Highest Level Signal Name In A Hierarchical VLSI Design; U.S. Patent Application Number 10/647,606, entitled System And Method For Determining Connectivity Of Nets In A Hierarchical Circuit Design; U.S. Patent Application Number 10/647,596, entitled System And Method Analyzing Design Elements In Computer Aided Design Tools; U.S. Patent Application Number 10/647,608, entitled System And Method For Determining Unmatched Design Elements In A Computer-Automated Design; U.S. Patent Application Number 10/647,598, entitled Computer Aided Design Systems And Methods With Reduced Memory Utilization; U.S. Patent Application Number 10/647,688, entitled System And Method For Iteratively Traversing A Hierarchical Circuit Design; U.S. Patent Application Number 10/647,769, entitled Systems And Methods For Establishing Data Model Consistency Of Computer Aided Design Tools; and U.S. Patent Application Number 10/647,607, entitled Systems And Methods For Identifying Data Sources Associated With A Circuit Design, the disclosures of which are hereby incorporated herein by reference.